with the thyristor shown in FIG. 2, so that the switching time can be shortened.

FIG. 5 illustrates a third embodiment of the double gate static induction thyristor in accordance with the present invention. In FIG. 5, elements and portions similar to those shown in FIG. 2 are given the same Reference Numerals and explanation thereof will be omitted. As seen from FIG. 5, the third embodiment comprises a plurality of thyristor units which are combined integrally and each of which substantially corresponds to the thyristor shown in FIG. 2 except that a plurality of shallow gate regions 51 and 61 are formed above and below each of the cathode and anode electrodes. This thyristor is for a large power.

The invention has thus been shown and described with reference to the specific embodiments. However, it should be noted that the invention is in no way limited to the details of the illustrated structures but changes and modifications may be made within the scope of the appended claims.

We claim:

1. A double gate static induction thyristor comprising a semiconductor substrate having first and second principal surfaces opposite to each other, a first gate region formed at the first principal surface of the semiconductor substrate, a first semiconductor region of a first conduction type formed on the first principal surface of the semiconductor substrate, a second gate region formed at the second principal surface of the semiconductor substrate, a second semiconductor region of a second conduction type opposite to the first conduction type and formed on the second principal surface of the semiconductor substrate, gate electrodes formed on the first and second gate regions, and main electrodes formed on the first and second semiconductor regions, portions of the semiconductor regions surrounded by the gate region forming a current path between the main electrodes, wherein the improvement is that each of the first and second gate regions has a first diffusion region positioned underneath the corresponding gate electrode in ohmic contact with the corresponding gate electrode, and a second diffusion region which extends from the first diffusion region toward a semiconductor region of the semiconductor substrate positioned between the main electrodes, a large part of the second diffusion regions is spaced away from the first diffusion region in a cross-sectional view along the direction of the current flow between said main electrodes, and is electrically connected to the first diffusion region, a diffusion depth of the first diffusion region from the surface in contact with the corresponding gate electrode being larger than that of the second diffusion region from the same level as the surface of the first diffusion region in contact with the corresponding gate electrode.

2. A thyristor as claimed in claim 1 wherein each of the first and second semiconductor regions is in the form of a mesa, and portions of the first and second gate regions exposed at the outside of the mesa-shaped first and second semiconductor regions are formed with the gate electrodes, the other portion of the first gate region being buried at a boundary between the substrate and the first semiconductor region, the other portion of the second gate region being buried at a boundary between the substrate and the second semiconductor region, said other portions of the first and second gate regions being respectively formed of impurity diffused regions having a diffusion depth smaller than that of said portions of the first and second gate regions formed with the gate electrodes.

3. A thyristor as claimed in claim 1 wherein each of the first and second semiconductor regions is in the form of a mesa, and all the first and second gate regions are exposed at the outside of the mesa-shaped first and second semiconductor regions.

4. A thyristor as claimed in claim 1 wherein the substrate includes a first semiconductor layer of the first conduction type and a second semiconductor layer of the second conduction type on the first layer with a p-n junction being formed between the first and second semiconductor layers, the first gate region and the first semiconductor region being formed at the first semiconductor layer, and the second gate region and the second semiconductor region being formed at the second semiconductor layer.

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